REMARKS

Claims 2 and 4 are pending herein. By the Office Action, claims 2-4 are rejected under 35 U.S.C. §103(a). By this Amendment, claim 2 is amended and claim 3 is canceled. Support for the amendments to claim 2 can be found in the specification at, for example, page 16, line 23 to page 17, line 8; page 26, lines 8-19; page 29, Table 1; and page 30, Example 2. No new matter is added. Applicants respectfully request reconsideration in view of the above amendments and the following remarks.

I. §103 Rejection

Claims 2-4 are rejected under 35 U.S.C. §103(a) over Nakano (US 6004866) in view of Takashi (EP 0928017). Claim 3 is canceled herein, rendering the rejection of that claim moot. Applicants respectfully traverse this rejection as to claims 2 and 4.

A. The Invention

The claimed invention is directed to bonded wafers having a base wafer bonded to a bond wafer, and where at least a chamfered part of the base wafer is mirror-polished. The claimed bonded wafers provide significant advantages over single wafers and bonded wafers of the prior art.

According to the prior art, bonded wafers were generally produced by either (1) use of grinding and polishing processes or (2) use of hydrogen ions or rare gas ions. See specification at page 1, last paragraph and page 3, line 5 to page 4, line 9. In the first method, one of the wafers, the bond wafer, is subjected to grinding and polishing processes to reduce its thickness to a desired thickness for subsequent fabrication of a device thereon. As a result, a SOI layer is formed on the other wafer, the base wafer. In the second conventional method, hydrogen ions or rare gas ions are implanted into a bond wafer to form a fine bubble layer. The bond wafer is then bonded to a base wafer. A portion of the bond wafer is then

delaminated by using the fine bubble layer as a cleavage plane, so that a SOI layer having a very thin and uniform thickness can be provided on the base wafer.

In each of the conventional methods, a bonded wafer is formed by bonding a base wafer and a bond wafer. As such, high flatness of each bonding surface is required. Thus, conventional practice has been to use conventional wafers in which one surface, the bonding surface, is mirror polished. See specification at page 5, lines 1-5 and page 7, lines 9-13.

Producing such bonding surfaces with a high flatness is difficult. One problem that must be addressed is the generation of particles, particularly at a chamfered part of a base wafer. In order to produce a thin film SOI wafer, such as a thin film SOI wafer having a film thickness of 0.1 ± 0.01 μm, it is necessary to apply processing steps such as alkali etching to advanced devices having very fine patterns or special structures. However, when alkali etching is applied to such structures, the problem of generation of particles becomes particularly important, especially at a chamfered part of a base wafer of the SOI wafer. Specification, page 8, line 22 to page 9, line 2. It is believed that such generation of particles arises from uneven shapes resulting from varying etching rates of various exposed orientations of the surface of the wafer. Page 9, lines 2-9.

The present inventors overcame the problems of the prior art by providing a bonded wafer having a base wafer, where a back surface of the base wafer is chemically etched or mirror polished, a chamfered part of the base wafer is mirror surface, and the base wafer is bonded to a bond wafer. In embodiments, the base wafer has a chemically etched back surface on which a maximal depth of pits is 6 μm or less, an average value of waviness is 0.04 μm or less and a power spectrum density is 0.5 to 10 μm^3 as measured by waviness having a wavelength of 10 mm. The present inventors have discovered that such a base wafer provides an SOI layer or silicon active layer that has extremely excellent thickness uniformity. Accordingly, a bonded wafer having the base wafer can be used for fabrication

of devices having fine patterns or special structures, and can suppress generation of particles even from a chamfered part. As a result, manufacturing yield and cost reduction are improved. Specification, page 17, line 24 to page 18, line 15 and page 27, lines 8-11.

B. Claim 2 is Patentable Over Nakano and Takashi

Claim 2 is directed to a bonded wafer having a base wafer wherein the base wafer has a chemically etched back surface on which a maximal depth of pits is 6 μm or less, an average value of waviness is 0.04 μm or less and a power spectrum density is 0.5 to 10 μm^3 as measured by waviness having a wavelength of 10 mm, and a chamfered part of the base wafer is mirror surface, wherein the base wafer is bonded to a bond wafer. Such a bonded wafer is not taught or suggested in Nakano and/or Takashi.

Nakano is directed to a method for manufacturing a bonded wafer comprising the steps of: mirror-polishing a surface of first and second substrates, bringing the mirror-polished surfaces of the substrates into contact with each other to join them, and subjecting the substrates to a heat treatment to firmly bond them. One of the surfaces of the first and second substrates prior to bonding, or one surface of the bonded wafer, is subjected to a polishing treatment for exerting little influence by irregularities on a rear surface of the one substrate or by a figure of a surface of a polishing plate that is in contact with the rear surface of the one substrate. Nakano at Abstract. Nakano thus generally discloses a method for manufacturing a bonded wafer, comprising mirror-polishing surfaces of two substrates, and joining the mirror-polished surfaces of the two substrates together. See Nakano at claim 1; Figs. 1A-1F.

Furthermore, at col. 6, lines 62-64, Nakano describes performing a polishing step on a surface of at least one of the substrates before bonding, or on a surface of the bonded wafer. Nakano also describes a double-side polishing step, where the front and rear surfaces of the wafer are polished at the same time. See col. 7, lines 11-59. This double-side polishing step

can be used to polish the base wafer or a bonded wafer. Col. 8, lines 41-44; Table 1. The Office Action argues that Nakano discloses all of the limitations of the claimed invention, except for the claimed maximal depth of pits, average value of waviness, and power spectrum density.

When a bonded wafer is produced according to the process of Nakano, the depth of pits and the waviness on a back surface of the base wafer may become small. However, and as admitted by the Office Action, Nakano does not disclose the claimed maximal depth of pits, average value of waviness, and power spectrum density. Nor does Nakano teach or suggest that such properties would necessarily result from the processing of Nakano. In fact, however, Nakano also fails to teach or suggest that a chamfered part of the base wafer is mirror-polished, as required by the claimed invention.

Takashi does not overcome the deficiencies of Nakano. Takashi is directed to semiconductor wafers. As indicated in the Office Action, Takashi discloses wafers having a maximal pit depth of 6 μm or less and an average value of waviness of 0.04 μm or less. See page 4, lines 44 and 45; paragraph [0034]. These properties are also shown in Takashi in Examples 2 and 3. Page 9, Table 1. Takashi discloses that the wafer can be formed by chamfering, lapping, etching, mirror polishing, and cleaning. See page 3, lines 1-4. The Office Action thus argues that when a bonded wafer is produced by the method of Nakano, but using the semiconductor wafers of Takashi, the result would be the invention of instant claim 2. Applicants disagree.

In particular, as described above, neither the wafers of Nakano nor Takashi have a chamfered part of the wafer that is mirror-polished. At least this feature is not taught or suggested by Nakano and/or Takashi. Even if a bonded wafer is produced using the semiconductor wafer of Takashi as a base wafer in the process of Nakano, the resultant product would not have a mirror-polished chamfered part, as neither reference teaches or

suggests to mirror-polish a chamfered part. As a result, the bonded wafer would generate particles, especially at the chamfered part, during subsequent etching processes, causing a lower process yield and higher process costs. The resultant bonded wafer would thus be different from the bonded wafer of the claimed invention, and would not solve the problems addressed by the claimed invention.

For at least these reasons, the claimed invention would not have been obvious over a combination of Nakano and Takashi. Thus, claim 2 is patentable over Nakano in view of Takashi. Reconsideration and withdrawal of the rejection are respectfully requested.

C. Claim 4 is Patentable Over Nakano and Takashi

Claim 4 is directed to a bonded wafer having a base wafer wherein at least a back surface and a chamfered part of the base wafer are mirror surface and the chamfered part of the base wafer is subjected to chamfering and mirror finishing, wherein the base wafer is bonded to a bond wafer. Such a bonded wafers would also not have been obvious over Nakano and Takashi.

As described above, Nakano teaches a base wafer or a bonded wafer that is mirror-polished by a single- or double-side polishing process. However, Nakano does not teach or suggest that a chamfered part of the wafer should be mirror-polished, or that such a mirror-polished chamfered part can reduce particle generation during subsequent steps. Nor does Nakano teach or suggest that such a mirror-polished chamfered part would accordingly improve manufacturing yield and reduce cost.

As also described above, Takashi also does not teach or suggest that a chamfered part of the base wafer is mirror-polished. Nor does Takashi teach or suggest that any benefits could be obtained by mirror-polishing a chamfered part.

In contrast, claim 4 specifically requires that the bonded wafer has a chamfered part of the base wafer that is mirror surface and the chamfered part of the base wafer is subjected

to chamfering and mirror finishing. These limitations are nowhere taught or suggested by the cited references, alone or in combination. Even if the wafer of Takashi was used in the process of Nakano, the result would still not have rendered obvious the claimed invention.

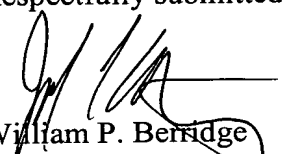
For at least these reasons, Nakano and Takashi would not have rendered obvious the bonded wafer of claim 4. Claim 4 is thus patentable over the cited references. Reconsideration and withdrawal of the rejection are respectfully requested.

II. Conclusion

In view of the foregoing amendments and remarks, Applicants submit that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the application are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,



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